Compact Multilayer Bandpass Filter Using Low-Temperature Additively Manufacturing Solution

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***Abstract*— This article presented an additively manufactured bandpass filter (BPF) based on a second-order stub-loaded resonator consisting of multimetal layer components. The proposed BPF is fabricated by a low-temperature (140°) additively manufactured electronics (AME) solution that can fabricate conductive and dielectric materials simultaneously with multimetal-layer and flexible interlayer distance. By reducing the interlayer distance, constant inductance and capacitance can be realized in smaller sizes, which helps to achieve device minimization. Taking advantage of this inkjet printing technology, a second-order multimetal layer resonator is proposed. To understand the principle of the BPF, an equivalent circuit with odd- and even-mode analysis is demonstrated. For verification, the frequency response of the circuit's mathematical model is calculated to compare with the electromagnetic simulation results. Good agreement can be achieved among the calculated, simulated, and measured results. The proposed BPF is designed at 12.25 GHz with a bandwidth of 40.8% and a compact size of 2.7 mm × 1.425 mm × 0.585 mm or $0.186\lambda g \times 0.098\lambda g \times 0.040\lambda g$, which is suitable for circuit-in-package applications in television programs, radar detection, and satellite communications.**

***Index Terms*— 3-D inkjet printing, additively manufactured electronics (AME), bandpass filter (BPF), low-temperature, multimetal-layer components, wide stopband.**

I. Introduction

With the rapid development of additive manufacturing technology, more and more multimaterial 3-D printers can fabricate conductive and dielectric materials simultaneously, which have demonstrated their capabilities in electronic device integration and 3-D packaging [1]–[5]. However, it is still a challenge for these 3-D printers to fabricate a seamless multimetal-layer in a single substrate. According to the open literature, multimetal-layer technologies have an outstanding advantage in device minimization such as low-temperature co-fired ceramic (LTCC) [6]–[10] or semiconductor technologies [11]–[13]. For example, Xu and Zhang [8] proposed a compact LTCC diplexer with high isolation. In [11], an on-chip miniaturized bandpass filter (BPF) is presented, which is based on a grounded center-tapped ring resonator with shunt capacitive loading. Although both designs demonstrated device minimization, these technologies are expensive and require complicated fabrication processes and longer production time. As an emerging technology, low-temperature additively manufacturing technologies have been applied in integrated electronic devices and packaging, such as electronic components [14], antenna arrays [15], terahertz lens [16], redistribution layers [17], combiner [18], transistors [19], and enzymatic biofuel [20].

In this article, a low-temperature additively manufactured electronics (AME) solution is introduced for BPF design, taking advantage of dual-materials (conductive and dielectric materials) printing, as shown in Fig. 1. Nano Dimension's DragonFly LDM system is used for AME designs with 4pL printer heads. This system simultaneously jets both dielectric and conductive inks, hence simultaneously creating multilayer conductive structures within a single dielectric substrate. Compared with LTCC and semiconductor technologies, the AME solution is flexible on electronic device fabrication with design freedom adjusting the interlayer distance. The printing process is carried out at a typical temperature of 140 °C in a standard ambient atmosphere. For proof-of-concept, a multilayer BPF with vertically integrated capacitors and inductors has been designed, analyzed, fabricated, and measured. Finite element electromagnetic (EM) field simulation analysis software, ANSYS High-Frequency Structure Simulator (HFSS), is used in the simulation, and the vector network analyzer (VNA) used in the measurement is a Keysight PNA N5225B.

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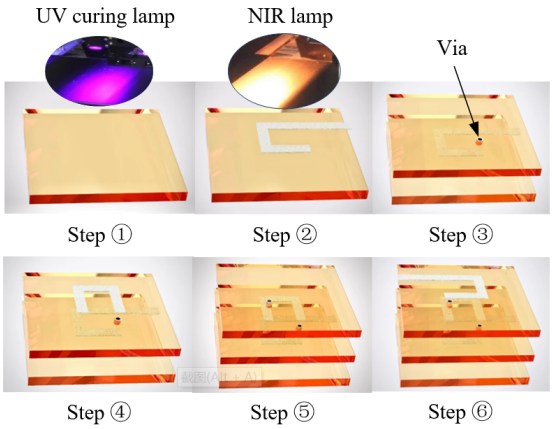

Fig. 1. Proposed low-temperature AME process.

II. Additively Manufactured Components for BPF Miniaturization

The printed BPF is composed of inductance and capacitance components. The proposed AME technique has the advantage of circuit miniaturization, which is demonstrated by using an inductor and a capacitor, as examples.

A. Miniaturized 3-D Spiral Inductor Using AME Process

As shown in Fig. 1, the fabrication procedure of a 3-D spiral inductor is demonstrated using the proposed low-temperature AME process. Silver nanoparticles and acrylate inks can be printed simultaneously in this AME process. During the manufacturing process, for *Step 1*, an ultraviolet (UV) lamp with a wavelength of 395 nm is used for curing the acrylate inks after they are ejected out from the nozzles. In *Step 2*, a metal strip line is printed on the acrylate layer. A near-infrared radiation (NIR) lamp with a wavelength of 0.75–1.4 μm and 140 °C to 170 °C process temperature is used to sinter the conductive inks. In *Steps 3–6,* acrylate and conductive inks are printed layer by layer to construct the 3-D spiral inductor. Vias can be printed simultaneously in the acrylate layer to connect metal strip lines in different layers, as depicted in *Step 3*. Where a via is desired, no dielectric ink is deposited. This via can remain through a via hole or can be filled with conductive silver nanoparticle ink. The fabrication is done layer by layer. Hence the silver is in the area where the filled via is being built, and the dielectric is around it. Taking advantage of the AME solution, designing 3-D components and devices would be flexible.

For vertical spiral inductors, the inductance can be calculated by

$$L = K\frac{\mu_0\mu_r N^2 A_e}{H} \tag{1}$$

where μ_0 is the permeability of free space, μ_r is the relative permeability of the material, N is the total number of turns; H is the total height of coil, A_e is the section area of the coil, and K is a coefficient that depends on the ratio of r (radius of the coil) to H. To investigate the relationship between the L and H, Fig. 2 demonstrates the comparison of simulated inductances with different dielectric-layer thickness h. When h drops from 0.15 to 0.05 mm, the inductance increases gradually. In addition, Fig. 2 shows the quality factor versus different values of h. With the decline of h, the inductance density increases, which means that a higher inductance value can be obtained with a lower profile and constant plane size. A drop in peak quality factor is observed because increasing inductance usually involves increasing magnetic layer thickness, which leads to higher eddy currents.

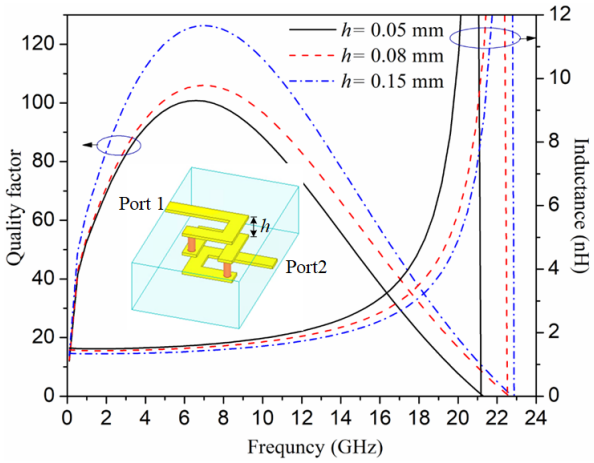

Fig. 2. Simulated inductances and quality factors of multilayer spiral inductors with different dielectric-layer thickness h.

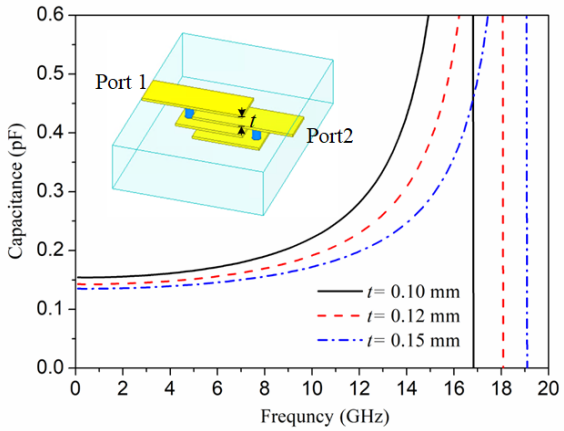

Fig. 3. Comparison of simulated capacitances of multilayer capacitors with different dielectric-layer thickness t.

B. Miniaturized Capacitors With Reduced Interlayer Distance

According to [21], for a multilayer capacitor, the capacitance "C" is given in the following equation:

$$c = \frac{\varepsilon_0\varepsilon_s S(n-1)}{t} \tag{2}$$

where ε_0 is the dielectric constant of free space, ε_s is the relative dielectric constant of the material, S is the effective area of the inner electrode. n is the number of inner electrodes, and t is the thickness of the dielectric layer.

Obviously, with the increase of the number of inner electrodes or raising the inner electrode effective area, the capacitance will grow. That is also the most common method to design a capacitor in previous literature. However, in this

article, the effect of the thickness of the dielectric layer is discussed. As shown in Fig. 3, with the decrease of dielectric-layer thickness t from 0.15 to 0.10 mm, capacitance increases significantly while the capacitor size keeps unchanged, consistent with (2). In other words, the adjustable interlayer distance can contribute to a smaller plane size and lower profile.

III. Multilayer BPF and Its Equivalent Circuit

A. BPF Configuration

In Fig. 4(a), the 3-D view of the proposed BPF is presented. Taking advantage of the proposed AME solution, the number of metal layers and the dielectric layer thickness among metal layers can be flexibly defined for circuit design. In this work, as shown in Fig. 4(b), five metal layers are employed to design the BPF, where layer 5 is used as the ground. The constructions of feeding lines and resonators are distributed from layer 1 to layer 4. The resonant part of the BPF consists of two $\lambda/4$ resonators, where three metal layers are stacked to form a compact capacitor. Two stepped-impedance stubs, located on layer 1 and layer 3, respectively, are loaded at the one-third point to improve the out-of-band suppression. Two up-raised grounds located at layer 3 are connected to the RF ground by 24 vias, respectively, to adjust the impedance match. Fig. 4(c) depicts the layout of the metal layers. Parameters of the proposed BPF are determined as follows (all in mm): $D_1 = 3.3, D_2 = 1.6, D_3 = 1.28, D_4 = 1.3, D_5 = 1.305, D_6 = 0.85, D_7 = 0.4, D_8 = 0.5, D_9 = 0.85, D_{10} = 0.425, D_{11} = 0.7, W_1 = 0.5, W_2 = 0.125, W_3 = 0.4, W_4 = 0.65, W_5 = 0.15, W_6 = 0.4, r_1 = 0.1$, and $g_1 = 0.7$. The dimension of BPF excluding feeding lines is 2.7 mm $\times$ 1.425 mm $\times$ 0.585 mm or 0.186 $\lambda g \times 0.098\ \lambda g \times 0.040\ \lambda g$, where λg is the guided wavelength at the center frequency. Fig. 4(d) shows the photograph of an additively manufactured prototype with testing accessories and structural details of the filter under a microscope.

B. Equivalent Lumped Component Circuit

To facilitate the analysis of the proposed multimetal layer BPF, an equivalent circuit based on the unfolded layout of the BPF is presented and discussed. Fig. 5 presents the equivalent lumped component (LC)-circuit model of the presented EM structure, where inductors and capacitors represent the high-impedance lines and the capacitive couplings, respectively. L_{Fi} $(i = 1, 2)$ denotes the self-inductances of the feeding lines. C_F is the capacitive coupling between the soldering area of the SMK connector and the ground. C_b represents the coupling capacitance between the feeding line and the resonator. C_p is the bypass capacitance of the feeding line to the ground. In addition, the source to load coupling is modeled by C_{S-L}. The inductors and capacitors of the resonators are L_1 and C_1, where L_1 and C_1 represent the parasitic inductor and the capacitance of this three-dimension interdigital capacitor, respectively. L_2 is the self-inductance of the quarter wavelength resonator. The loaded stepped-impedance is represented by C_2, L_3 and C_3, L_4. C_2, L_3 denotes the low-impedance segment. The C_3 and L_4 denote the high-impedance segment.

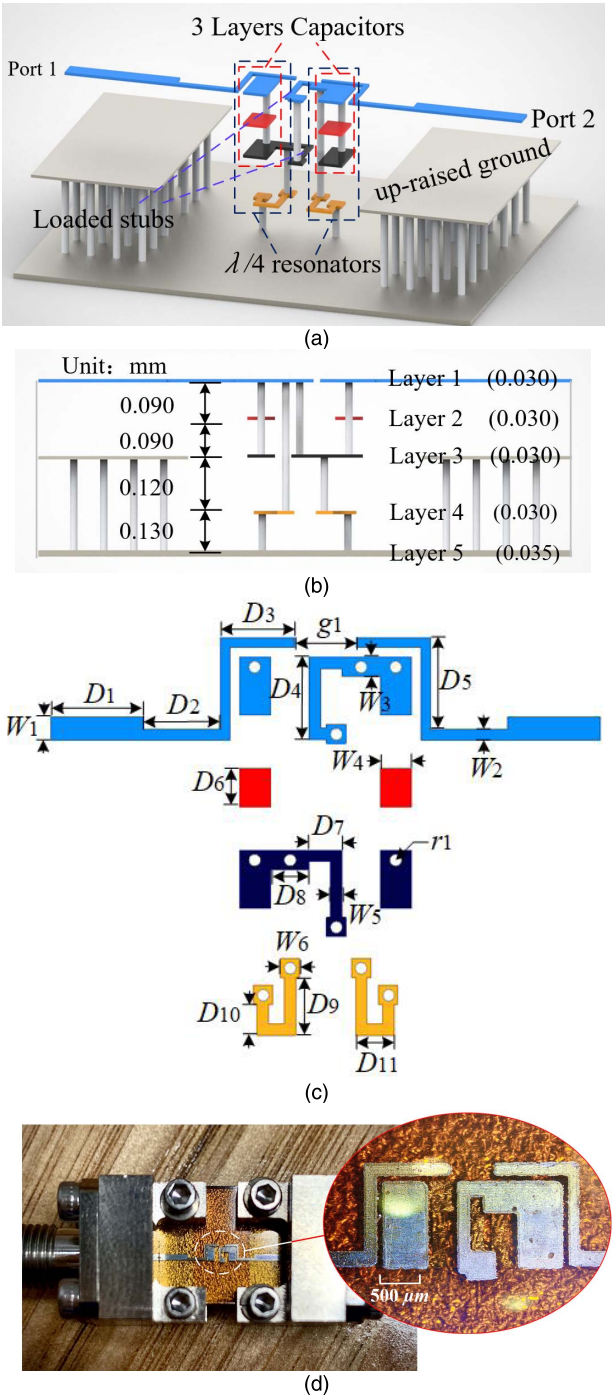

Fig. 4. (a) 3-D view, (b) side view, (c) layout of each layer, and (d) photograph of the 3-D printed BPF with testing accessories and structural details of the filter under microscope.

C. Analysis of Equivalent LC-Circuit Model

For circuit analysis, an equivalent LC-circuit of resonators is depicted in Fig. 6(a). Since the two resonators are symmetrical about AA′, odd-and even-mode circuits can be obtained, as shown in Fig. 6(b) and (c).The loop equation method is used for circuit analysis, of which the loop currents I_i $(i = 1, 2, 3, 4)$ are marked in Fig. 6(b) and (c). The expressions of input admittance are listed to calculate the resonant frequencies of transmission poles (TPs) and transmission zeros (TZs).

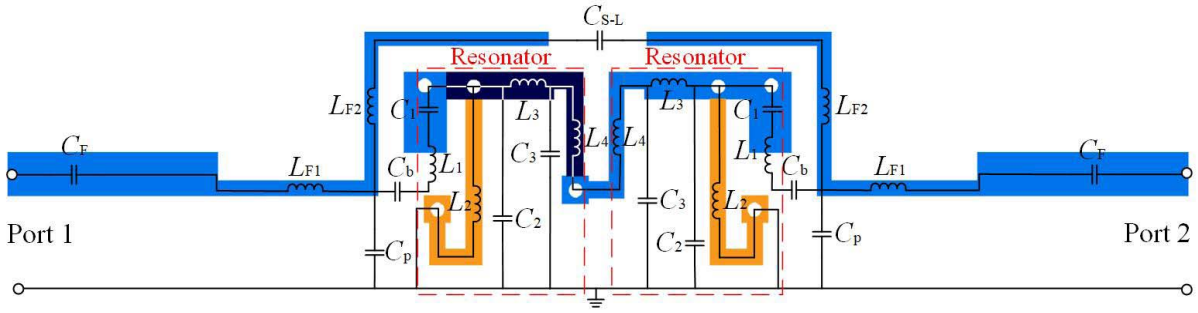

Fig. 5. Equivalent LC-circuit model based on unfolded layout of the proposed BPF (derived from Fig. 4(a) for illustration of the LC components).

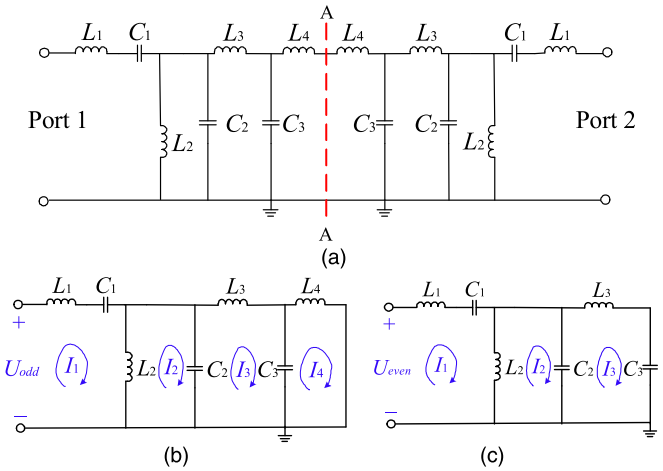

Fig. 6. (a) Equivalent circuit of the resonators and its (b) odd-and (c) even-mode equivalent circuits.

Applying Kirchhoff's voltage law (KVL) to the odd-mode equivalent circuit in Fig. 6(b), the voltage equations of the four loops are expressed as

$$\frac{I_1}{sC_1} + sL_1I_1 + sL_2(I_1 - I_2) - U_{\text{odd}} = 0 \tag{3}$$

$$\frac{(I_2 - I_3)}{sC_2} + sL_2(I_2 - I_1) = 0 \tag{4}$$

$$\frac{(I_3 - I_2)}{sC_2} + sL_3I_3 + \frac{(I_3 - \mathrm{I}_4)}{sC_3} = 0 \tag{5}$$

$$sL_4I_4 + \frac{(I_4 - I_3)}{sC_3} = 0. \tag{6}$$

Similarly, applying KVL to the even-mode equivalent circuit in Fig. 6(c), the voltage equations of the three loops are expressed as

$$\frac{I_1}{sC_1} + sL_1I_1 + sL_2(I_1 - I_2) - U_{\text{even}} = 0 \tag{7}$$

$$\frac{(I_2 - I_3)}{sC_2} + sL_2(I_2 - I_1) = 0 \tag{8}$$

$$\frac{(I_3 - I_2)}{sC_2} + sL_3I_3 + \frac{I_3}{sC_3} = 0 \tag{9}$$

where U_{odd} and U_{even} denote the input voltages of odd-and even-mode circuits, respectively. s is a complex variable in proportion to angular frequency ω. Therefore, the relationships between input voltages and input admittances in Fig. 6(b) and (c) can be written as

$$Y_{\text{odd}}(s) = \frac{I_{1\_\text{odd}}(s)}{U_{\text{odd}}(s)} = \frac{I_{1\_\text{odd}}(j\omega_{\text{odd}})}{U_{\text{odd}}(j\omega_{\text{odd}})} \tag{10}$$

$$Y_{\text{even}}(s) = \frac{I_{1\_\text{even}}(s)}{U_{\text{even}}(s)} = \frac{I_{1\_\text{even}}(j\omega_{\text{even}})}{U_{\text{even}}(j\omega_{\text{even}})} \tag{11}$$

where ω denotes angular frequency, and j is a pure imaginary unit number. Using MATLAB, the expression of input admittances consists of complex variable s and lumped LC-elements can be deduced by solving (2)–(11). Since $\omega = 2\pi f$, the frequencies f_{odd} and f_{even} (corresponding to odd-and even-mode) can be calculated when $Y_{\text{odd}}(j\omega) = 0$ and $Y_{\text{even}}(j\omega) = 0$, respectively. Meanwhile, the TZs can be determined when $Y_{\text{odd}}(j\omega) = Y_{\text{even}}(j\omega)$. For verification, the equivalent LC-circuit is optimized to match the finite element EM field simulation result of the EM structure. As shown in Fig. 7(a), the simulated results of equivalent LC-circuit carried by ADS are illustrated. Good agreement can be obtained between the calculated results of LC-circuit and simulated results of the EM structure. Substituting the obtained values of lumped elements in equivalent circuit: $L_1 = 0.016$ nH, $L_2 = 0.589$ nH, $L_3 = 0.725$ nH, $L_4 = 1.247$ nH, $C_1 = 0.345$ pF, $C_2 = 0.18$ pF, $C_3 = 0.11$ pF into (12) and (13), one TZs f_{zi} $(i = 1)$ and two TPs $f_{pi}(i = 1.2)$ can be obtained in the frequency range of 0–35 GHz through the calculations. Finally, the estimated TZs and TPs are marked in Fig. 7(a) as well. Compared with the simulated results of TZs and TPs: $f_{z1} = 19.85$ GHz, $f_{p1} = 11.31$ GHz, and $f_{p2} = 13.18$ GHz, the calculated results agree well with the simulated ones. In addition, to improve the skirt selectivity, (source-load) S-L coupling is induced by adding a capacitor between two ports, as shown in Fig. 7(b). The locations of the TZs are dependent on the mixed EM coupling coefficient between the two resonators and the (source–load) S–L coupling construction. Since these two resonators of the BPF are connected by via, which results that the magnetic coupling is larger than the electric one. Therefore, a TZ would be excited at the upper (magnetic-dominant coupling) stopband (TZ_2). As shown in Fig. 8(a), the frequency response of the coupled resonators against spacing D_7 is depicted, which shows the variation of the EM coupling between the two resonators. Lower-band TZ (TZ_1) and upper-band TZ (TZ_2) are marked in the picture. By tuning D_7, the location of the TZ_2 can be adjusted at the upper stopband, which significantly

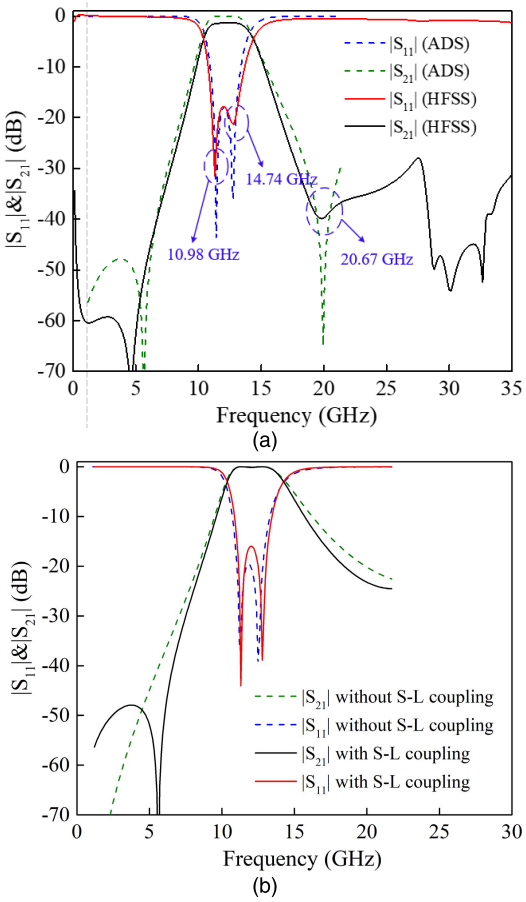

Fig. 7. Simulated frequency responses of (a) BPF (by HFSS) as well as the equivalent LC-circuit in Fig. 6 (by ADS) and (b) simulated frequency responses of the BPF with or without S-L coupling.

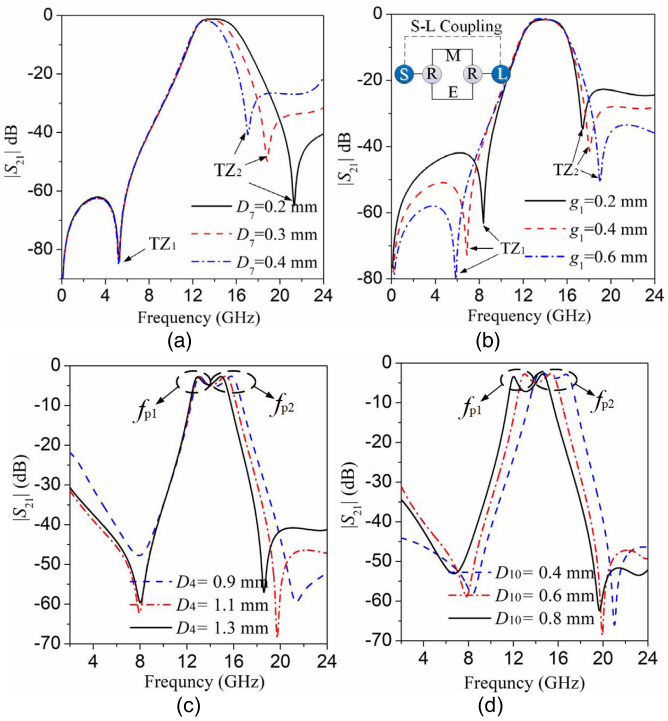

Fig. 8. Simulated frequency responses against (a) D_7, (b) g_1 with coupling topology inserted, and (c) D_4 and (d) D_{10}.

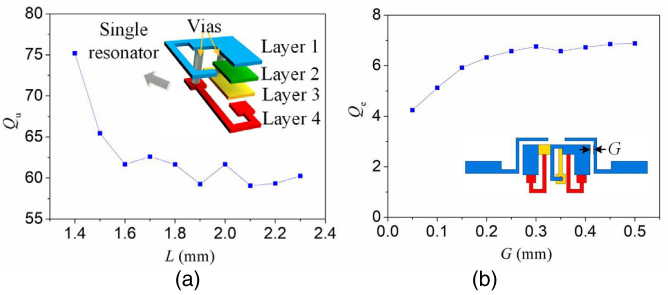

Fig. 9. (a) Simulated unloaded Q_u of the proposed single resonator against a different L (b) and extracted external quality factors Q_e against a different coupling gap G.

enhances the out-of-band attenuation of the proposed filter, while the TZ_1 keeps unchanged.

In addition, the simulated frequency response against g_1 is given for the TZ created in the low-band (TZ_1), as shown in Fig. 8(b). When g_1 decreases from 0.3 to 0.1 mm, the TZ_1 increases from 5.88 to 8.37 GHz, whereas the TZ_2 changes slightly without affecting the filter bandwidth. The closer the TZs to the passband, the better the frequency selectivity can be achieved.

For the frequency response of the TPs, by solving $Y_{\text{odd}}(j\omega) = 0$ and $Y_{\text{even}}(j\omega) = 0$, it can be found that the even-mode resonant frequency f_{even} is the function of L_4, while f_{odd} is the function of both L_2 and L_4. L_2 and L_4 correspond to the length of D_4 and D_{10} in the EM structure, respectively. For validation, the simulated responses against D_4 and D_{10} are shown in Fig. 8(c) and (d). When D_4 rises from 0.9 to 1.3 mm, f_{p1} keeps constant while f_{p2} decreases gradually. Besides, with the development of D_{10}, f_{p1} and f_{p2} decline simultaneously. The variations are consistent with the analysis and verify that the bandwidth and center frequency can be flexibly designed.

The unloaded quality factor of the resonators is important for filter performance. In Fig. 9(a), for a single resonator used in the proposed BPF (center frequency = 12.25 GHz), the simulated unloaded Q-factor versus the length $L = D_9 + D_{10} + D_{11}$ is presented. According to Fig. 9(a), when L increases, the unloaded Q_{u} decreases due to dielectric and conductor losses. Besides, the external quality factor Q_e with varied coupling gap G is depicted in Fig. 9(b). When G increases from 0.05 to 0.5 mm, a higher Q_e of the filter can be obtained, which causes a decrease of the bandwidth.

D. Suppression of Third Harmonic and Wide Stopband

Fig. 10(a) shows the structure of the quarter-wavelength resonator used in the proposed BPF. A short-circuited stepped impedance stub is loaded at the trisection point of this resonator closing to the input terminal. The electrical lengths of the quarter-wavelength transmission line are referred to as θ_1 and $2\theta_1$. The short-circuited stub position can be defined by analyzing the voltage distributions of the fundamental mode and the third harmonic to improve the out-of-band suppression. It is obvious that the shorted terminal of the quarter-wavelength resonator is the common voltage zero point of the fundamental mode and the third harmonic mode,

TABLE I
COMPARISON WITH SOME OTHER BPF

Ref.	f_0 (GHz)	*FBW (%)	Number of TZs	Filter order	Stopband (GHz)	ε_r/tanδ	Size (mm^2)/ (λ_g^2)	Thickness (mm)/ (λ_g)	Fabricated process
[2]	1.6	22	0	4	0.25 f_0 (20dB)	2.75/0.015	20×83/0.177×0.735	3.6/0.032	Additive manufacturing
	2.45	12	0	4	0.16 f_0 (20dB)	2.35/0.02	11.15×50/0.140×0.626	3.6/0.045	
[11]	33	42.4	0	1	1.58 f_0 (20dB)	N.A.	0.11×0.28/N.A.	N.A.	0.13-μm (Bi)-CMOS
[12]	59.5	21.68	2	2	N.A.	N.A.	0.240×0.225/0.144×0.135	N.A.	0.18-μm CMOS
[24]	4.3	44.2	1	3	2.6 f_0 (20dB)	5.9/N.A.	12×6 /0.418×0.0209	1/0.035	LTCC
This work	12.25	40.8	2	2	1.9 f_0 (20dB)	2.75/0.025	2.7×1.425/0.186×0.098	0.508/0.04	AME solution

*FBW= fractional Bandwidth

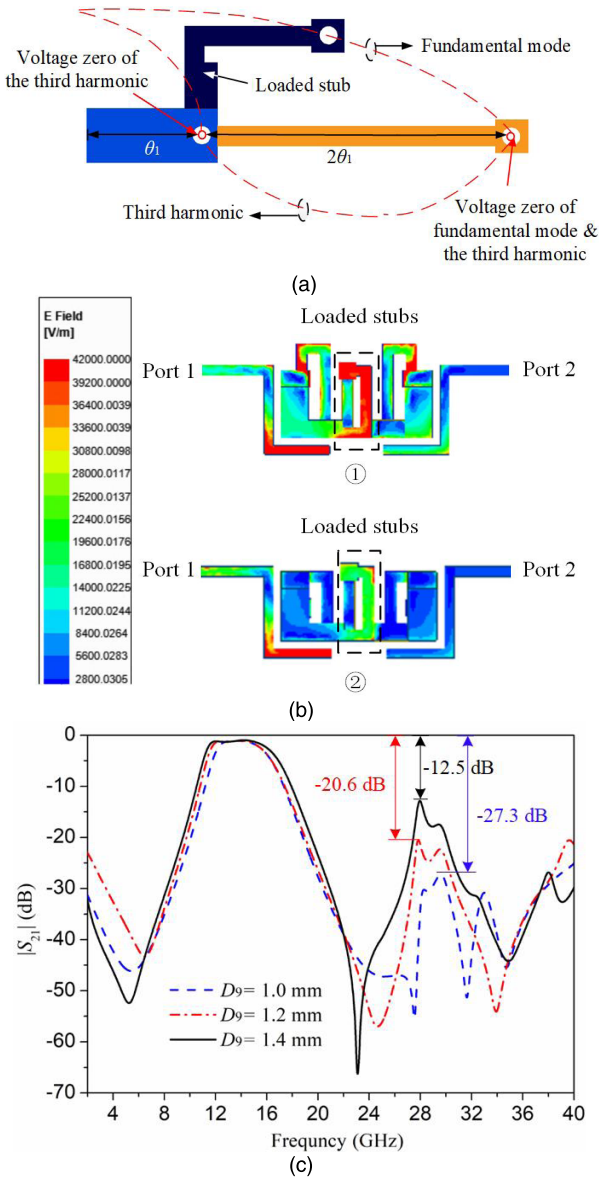

Fig. 10. (a) Voltage distribution of the quarter-wavelength resonator used in the proposed BPF. (b) Electric filed distribution of the proposed filter at the resonate frequency of third harmonic mode when ① $D_9 = 1.4$ mm and ② $D_9 = 1$ mm. (c) Simulated $|S_{21}|$ against D_9.

while the trisection points near the input terminal are the zero-voltage point only for third harmonic modes. When the shorted stub is located at the zero-voltage point of the third harmonic mode, the third harmonic mode signal will not get through the resonator, as shown in Fig. 10(b). Thus,

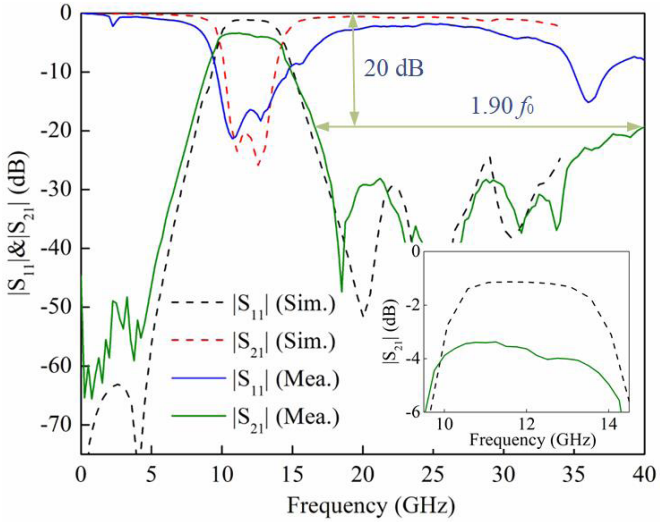

Fig. 11. Simulated and measured frequency response with a zoomed-in view of the passband insert loss of the AME printed BPF.

out-of-band suppression can be developed by adjusting the location of the loaded stub. In Fig. 10(c), with the decrease of D_9 from 1.3 to 1 mm, the loaded stub approaching the zero-voltage point of the third harmonic mode gradually, and the out-of-band suppression is improved from 12.5 to 27.3 dB.

IV. MEASUREMENT RESULT

The performance of the designed BPF is measured from 1 up to 35 GHz. Good agreement between the simulated and measured results is observed in Fig. 11. The dielectric constant of the additive manufactured substrate is 2.75, and the loss tangent is 0.025. [22], [23]. The conductivity of the silver film is 3.15×10^6–$2.52 \times 10^7\sigma$ (S/m) at 20 °C. As demonstrated in Fig. 11, compared with the simulated results achieved by HFSS, the measured insertion loss and return loss are 3.42 and 16.65 dB at the center of 12.25 GHz, respectively. In the measurement, the connection between the SMK connector and the filter will cause interconnection loss, which will lead to a deteriorated insertion loss. At the same time, the error of the thickness in the manufacturing process is also the reason for a deteriorated insertion loss. A 3-dB bandwidth is achieved from 9.58 to 14.57 GHz with an FBW of 40.8%. Two TZs located at 3.51 and 18.51 GHz that can improve the selectivity are generated. In addition, due to the loaded short-circuited stepped impedance stub the upper stopband with more than 20-dB rejection level is extended to 23.24 GHz (from 16.65 to 39.89 GHz) or 1.90 f_0. As can be

seen, the designed BPF working at 12.25 GHz has the merits of multiple TZs and poles, a compact size, and a wide stopband that can be assigned to television programs or be utilized in radar detection and satellite communications.

Table I shows the comparison of the proposed BPF with other state-of-the-art BPFs fabricated with different fabricated processes. Compared with [2], the BPF proposed in our work has a larger FBW, two flexibly designed TZs, a wider stopband, and a smaller size. In addition, compared with traditional multilayer processes, such as CMOS and LTCC technology, the proposed BPF has a good FBW, high-band and low-band TZs, a good stopband, and a competitive footprint. Furthermore, AME solution used in this article has the advantages of a low-cost and short processing cycle.

V. Conclusion

In this article, a low-temperature AME technology for multilayer 3-D BPF design is presented. Equivalent circuits and KVL are used for analyzing the frequency response of the printed BPF. The proposed additive manufacturing process functions at a typical temperature of 140 °C in a standard ambient atmosphere. Good agreement among the calculated, EM simulated and measured results validate the feasibility of the proposed AME solution for miniaturized BPF design. The proposed AME solution has great potential in circuit-in-package applications.

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